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# A Clock-gating-based Energy-efficient Scheme for ONUs in Real-time IMDD OFDM-PONs

Junjie Zhang, Jiahe Zhao, Hanzi Huang, Nan Ye, R. P. Giddings, Zhengxuan Li, Deli Qin, Qianwu Zhang, and J.M.Tang

**Abstract**—A clock-gating-based energy-efficient scheme is proposed, for the first time, for applications in optical network units (ONUs) accommodated by orthogonal frequency division multiplexing passive optical networks (OFDM-PONs) based on intensity modulation and direct detection (IMDD). In the operation of a conventional downlink OFDM-PON, each ONU has to perform the demodulation in physical layer for all the received OFDM frames, regardless the received frames belong to the ONU or not. To improve the ONU's energy consumption efficiency, in this paper, frame identification and clock control modules are introduced into each ONU, where the former is to distinguish whether a received frame belongs to the ONU or not, and the latter is to control the operating clock of the OFDM demodulation module according to the frame identification output. As a result, when a non-local frame arrives, the operating clock is set to a low value by the clock control module to deactivate the OFDM demodulation module in order to avoid unnecessary power consumption of the module. Experiments are undertaken in a real-time IMDD OFDM-PON platform, and measured results show that 51% energy consumption of a field programmable gate array (FPGA) chip embedded in the ONU can be saved compared with its conventional counterpart for downlink unicast scenarios.

**Index Terms**—Clock-gating, frame identification, energy-efficient, real-time, OFDM-PON.

## I. INTRODUCTION

THE rapidly expanded information and communication technology (ICT) consumes 8% of the global electricity, of which 70% is taken by the core and access network equipment [1], developing energy-efficient equipment and corresponding protocols is thus vital for reducing the overall data network energy consumption. To achieve such an objective, passive optical networks (PONs) are widely considered to be a promising solution because of their less energy consumptions and high signal transmission speeds. Due to their performance robustness to chromatic dispersion and high spectral efficiency, over the past 15 years, orthogonal frequency division multiplexing passive optical networks (OFDM-PONs) have

been extensively investigated for applications in next-generation optical access networks (NG-PONs) [2]. However, OFDM-PONs consume more energy than other PONs because OFDM requires high speed analogue-to-digital/digital-to-analogue converters (ADCs/DACs) and digital signal processing (DSP) chips [3]. As such, it is greatly important to explore new techniques capable of delivering highly energy-efficient optical OFDM-PONs in order to accelerate their practical implementation.

To address the aforementioned bottleneck challenge, various energy-saving OFDM-PON schemes have been proposed: by taking into account the fact that the fast Fourier transform/inverse fast Fourier transform (FFT/IFFT)-embedded high speed OFDM-PON systems takes >80% of the total FPGA logical usage [4] and consumes ~50% of the dynamic power of a FPGA chip [5], reducing the FPGA logical usage is thus a straightforward approach for lowering OFDM-PON's power consumption. According to this strategy, Bouziane et al. [6] have studied the effect of FFT size on the performance and power consumption of real-time optical OFDM transceivers, and their results suggest that a large FFT size requires a high bit precision and thus consumes more power. On the other hand, for the FFT/IFFT operation of a fixed size, Kimura et al. [7] have also shown that a reduced precision of the FFT/IFFT operation can reduce the chip power consumption. This leads to their proposition of an energy-saving technique by dynamically controlling the precision of the FFT/IFFT operation according to signal-to-noise ratios (SNRs). Further improvements in the energy consumption efficiency of OFDM-PONs based on intensity modulation and direct detection (IMDD) are also achievable when the dynamic SNR management is conducted in conjunction with adaptive modulation [8]. Furthermore, Hu et al. [3] have proposed a time-domain interleaved OFDM technique, which can save 17.1% and 26.7% energy by setting the sampling rate and FFT size ratio at 1/2 and 1/4, respectively. Finally, by analyzing the FFT/IFFT DSP operation dynamic range and their corresponding FFT/IFFT stage-dependent precision, we have

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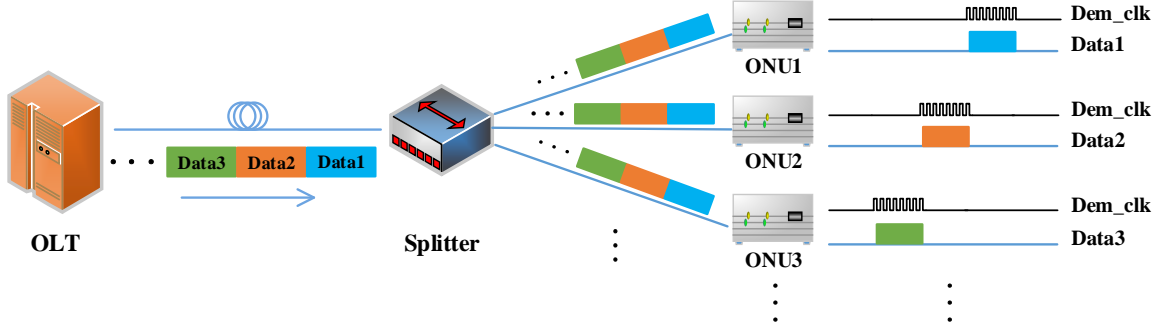


Fig. 1. Clock-gating-based energy-saving scheme for OFDM-PONs.

proposed and experimentally verified a minimum bit resolution map for the full-parallel pipelined 64-point FFT [9], and an analytical solution has subsequently been derived in [10], which significantly eases the practical utilization of the bit resolution map as sophisticated numerical simulations are no longer needed for a specific application scenario.

Apart from the abovementioned effort in making the OFDM-associated core FFT/IFFT operation more power efficient, in the network layer, several energy-saving schemes based on sleep-mode, doze-mode and dynamic bandwidth allocation (DBA) algorithm can also be used in the OFDM-PONs in low traffic load situations [11], [12]. For example, Zhang et al. [11] have proposed an energy-efficient OFDM-PON and achieved a ~40% energy efficiency improvement by using dynamic bandwidth allocation and adaptive sleep-mode control based on a bidirectional-centralized algorithm. However, due to the required change to the transceiver operation mode status, such a technique is not suitable for high traffic loads because of the difficulty in rapidly recovering from an energy-saving operation mode to an operation mode in a short time.

To deal with the above technical problem for practical use in high traffic load scenarios, selective physical layer frame reception has been proposed [13], where a high-precision frame recognition module is required to operate all the time in order to perform the desired frame identification in the physical layer. Li et al. [13] have used orthogonal pseudorandom (PN) sequences to identify the destinations of received frames. To avoid the utilization of extra overheads, Wu et al. [14] have embedded frames' destinations in their short training sequences (STSs). Both of these two schemes set ONUs to the standby mode when the destinations of the frames do not match the ONUs. In addition, in order to further reduce the complexity of the frame recognition process, in our previously published work [5], a simple frame logical link identification (LLID) based on amplitude decision in the time domain has also been proposed and verified in a FPGA-based real-time IMDD OFDM-PON platform. By setting the toggle rate of the demodulation module to zero when the recognized LLID does not match with the targeted ONU, 25.1% energy consumption can be saved.

However, considering the fact that the clock of the demodulation module in [5] still operates all the time, to further minimize the FPGA chip power consumption, in this paper, a clock-gating technique is proposed to control the clock of the OFDM demodulation module according to the recognized ONU LLID. In the proposed technique, when a local frame arrives,

the clock of the demodulation module is activated to ensure that the local frame is demodulated, otherwise, the clock is deactivated to save energy. The unique advantages associated with the clock-gating technique are summarized as following:

- 1) *Easy use and great simplicity.* Based on the simple, highly accurate, time domain ONU LLID recognition method presented in our previous work [5], only a single clock-gating module, termed BUFGCE for the Xilinx FPGA adopted in this paper, is used to enable/disable the clock for the OFDM demodulation module at the receiver.
- 2) *Extreme fine granularity control of the operation clock.* In this paper, by introducing a new frame alignment module to realign the considered 32-parallel ADC sampled data into a regular order, i.e., the first data enters the OFDM demodulation is always set at the initial index, a fixed pipeline delay for the real-time OFDM demodulation with the 4GS/s@12bit ADC is realized. Thus, based on the time-domain ONU LLID recognition and the inactiveness of the operating clock through the fixed pipeline delay of the OFDM demodulation module for received non-local frames, the realization of OFDM frame control of the OFDM demodulation is demonstrated and experimentally verified in this paper. In this paper, the control granularity of the operating clock is ~2  $\mu$ s.
- 3) *Experimental verification of the high accuracy and robustness of the clock-gating technique.* Based on a FPGA-based real-time IMDD OFDM platform, experimental results show that the proposed clock-gating technique results in negligible transceiver bit error ratio (BER) performance degradations and that the clock-gating technique is transparent to various transceiver design parameters including signal modulation format, received optical power and number of the OFDM symbols per frame.
- 4) *Experimental verification of a significantly large energy efficiency.* In downlink unicast OFDM PON systems, our real-time FPGA-based IMDD OFDM experimental results show that 51% and 29% power consumption of a FPGA chip at the receiver side can be saved compared with their conventional counterparts without the clock-gating technique and our previous toggle-rate based scheme [5] respectively.

## II. OPERATION PRINCIPLE OF THE CLOCK-GATING BASED ENERGY-SAVING SCHEME IN REAL-TIME IMDD OFDM-PONS

For the operation of each ONU in a conventional downlink OFDM-PON, the OFDM demodulation has to be always operational at physical layer to process all received analogue signals to identify, at MAC layer, whether a frame belongs to this ONU or not, as such the OFDM demodulation module at the receiver side wastes a lot of energy even only a few frames belong to the ONU. If the frame identification at physical layer is excluded before frame demodulation, and a decision of whether or not the frame demodulation process is needed is made according to the results of frame identification, a lot of energy can thus be saved. In this paper, a clock-gating based energy-saving scheme is proposed, where the following frame identification process is performed: when a local frame arrives, the demodulation module operates normally, otherwise, the clock of the demodulation module is deactivated to save energy. Obviously, the proposed scheme can save more energy compared with our previous work because the clock in [5] still operates when the toggle rate is set to zero.

The clock-gating based energy-saving scheme for the OFDM-PON is shown in Fig. 1. Assuming that the destinations of Data1, Data2 and Data3 are ONU1, ONU2 and ONU3, respectively, in a downlink unicast situation, the downstream data from the optical line terminal (OLT) is broadcast to each ONU. In a conventional OFDM-PON, all ONUs perform the demodulation operation for all received data and the clock of the demodulation module is always operating. However, in our proposed clock-gating-based energy-saving scheme, the clock of the demodulation module, named “Dem\_clk”, in ONU1 remains deactivated until Data 1 arrives, and the demodulation of Data1 is performed during the “Dem\_clk” signal duration. After data demodulation, the “Dem\_clk” signal is set to low immediately. The same procedure applies for both ONU2 and ONU3.

## III. REALIZATION OF THE CLOCK-GATING-BASED ENERGY-SAVING SCHEME IN REAL-TIME IMDD OFDM-PONS

### A. Overall descriptions of DSP blocks for realizing the real-time OFDM receiver incorporating the clock-gating technique

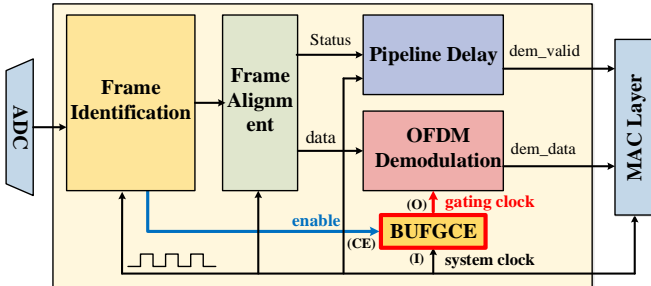


Fig. 2. Real-time OFDM receiver DSP blocks with clock-gating control.

The DSP blocks of a real-time OFDM receiver with the clock-gating control for baseband signal processing is depicted in Fig. 2, where only the major modules are shown, which perform functions including frame identification, frame alignment, pipeline delay, BUFGCE (clock-gating module) and OFDM demodulation. The whole FPGA-based real-time

OFDM receiver operation is performed in two separate clock domains, i.e. system clock domain and gating clock domain. Only the OFDM demodulation modules including the FFT, channel estimation/equalization and de-mapping operate in the gating clock domain, and all the others operate in the system clock domain that are kept working all the time. From Fig. 2, it can be seen that the key technical challenge associated with the proposed clock-gating-based energy-saving scheme is to achieve precise frame recognition and accurate gating clock control.

The frame identification module is used to identify whether the received OFDM frames at the receiver side belong to the targeted ONU or not, and the recognition of the ONU's LLID (inserted in the frame structure and used to indicate which ONU the frame is sent to) is realized after the OFDM symbol synchronization function (not shown in Fig. 2), which is located between the ADC and the frame identification module. It should be noted that both symbol synchronization and frame identification can be undertaken using amplitude decision in the time domain because of the experimentally verified stable physical channel characteristic of the IMDD OFDM PON system [5]. Moreover, these two functions should operate all the time at the system clock in order to obtain the correct ONU LLID from the continuously sampled ADC data. The result of frame identification is sent to the BUFGCE module by one bit “enable” signal (“1” represents a local frame and “0” indicates a non-local frame).

The gating clock is realized by BUFGCE in a Xilinx FPGA used in our platform discussed in section IV. BUFGCE is a global buffer with a clock enabler. It has an input port I, an enabler port CE and an output port O. The BUFGCE output is only available when the enabler port CE is active (high). Port I, port CE and port O are connected with the system clock, the “enable” signal is produced from the frame identification module and gating clock, respectively. When a local frame arrives, the “enable” signal is set to “1” and the gating clock is turned on and operates normally with a frequency equal to the system clock. And then the OFDM demodulation module including the FFT, channel estimation/equalization and de-mapping, operates to realize the demodulation of the received local frame. If the “enable” signal is set to “0”, the gating clock is set to low and the OFDM demodulation module stops operating to keep the state of the lowest power consumption.

In addition, considering the fact that the operation frequency of a FPGA chip is typically several hundreds of Mega Hz, while a representative ADC sampling frequency is > GHz, therefore multi-parallel processing must be applied to realize the high throughput of an OFDM receiver. To simplify the high-speed data processing for OFDM demodulation, a frame alignment module is introduced to realign the sampled ADC data into a regular order, i.e., the first data of an OFDM frame is always in the first branch of the 32 parallel pipeline. The newly reordered ADC data from the frame alignment module is passed to the OFDM demodulation module and detailed illustrations of the signals from the frame alignment for practical cases can be found in Fig.4. The frame alignment module greatly reduces the

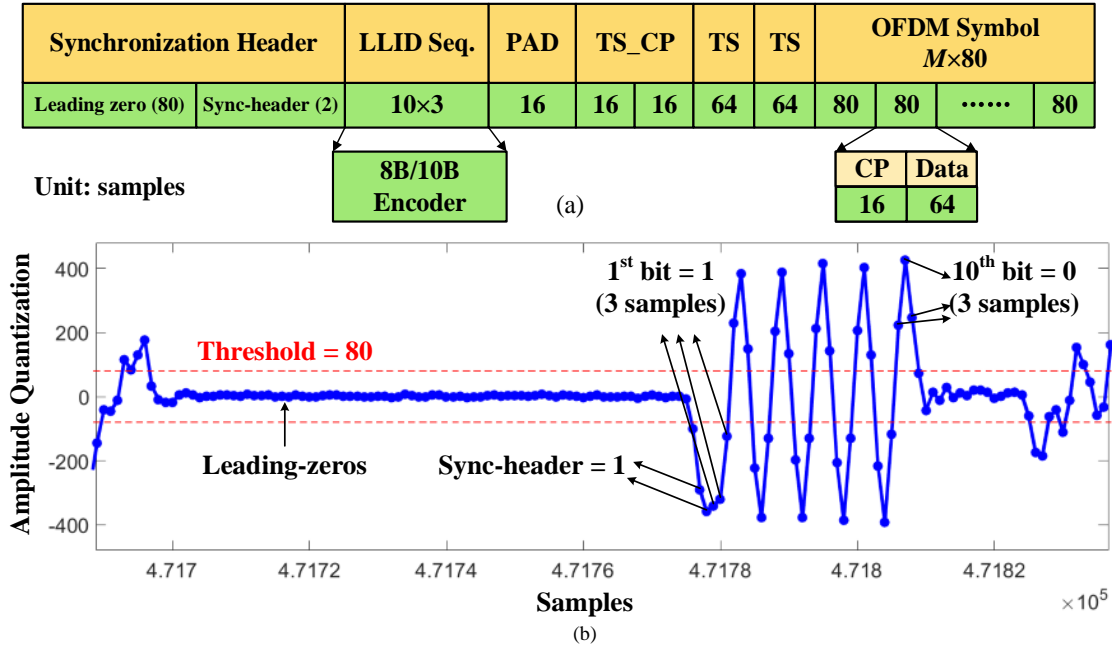


Fig. 3. (a) Time-domain OFDM frame structure. (b) Time-domain waveform of LLID with the value of “1010101010” (ROP=-10dBm).

FPGA/ASIC (application specific integrated circuit) realization complexity of the high-parallel and high-throughput baseband signal processing module. Considering the high regular data format and the pipelined processing technique adopted to realize the high speed OFDM demodulation where the fixed pipeline delay varies between different OFDM demodulation strategies, another additional advantage of using the frame alignment module is to make the pipelined processing delay of the OFDM demodulation module to be fixed, i.e.  $K$  clocks delay ( $K$  is 55 in our design, as shown in Fig.6) for the practical FPGA design which makes the control of the enable signal for the clock-gating module very simple.

Moreover, in order to avoid any unstable or incomplete signals, which may occur due to gating clock switching, to be processed by higher-layer functions, a pipeline delay module operating in the system clock domain is introduced to produce a frame indication signal (“dem\_valid” signal) to indicate the location of the demodulation results (“dem\_data” signal) of the local frames, because the fixed delay for the OFDM demodulation is achieved in this paper.

#### B. Realization of highly accurate ONU LLID recognition in the time domain with amplitude decision

In order to power-efficiently identify the ONU LLID with high accuracy and low DSP complexity from a continuously sampled ADC data, in this paper, both the symbol synchronization and LLID identification are realized with amplitude decision in the time domain, which has been successfully used in our previous work [5], [15] and its computational complexity is the lowest because only comparators are used.

In addition, for the integrity of the paper, the adopted frame structure and the corresponding time domain signal of the frame are shown in Fig. 3, which are similar to those reported in our previous work [5]. The synchronization header, which is used for symbol synchronization, consists of an 80-sample leading-

zeros and a 2-sample sync-header. For a specific FPGA implementation, the number of the leading zeros is dependent on FFT sizes, physical channel characteristics and processing parallelism. In general, the size of the leading zeros should be greater than the FFT size in order to decrease any misjudgments induced by the transmitted OFDM data. The quantized amplitude values of the sync-header are set to be 1200 to eliminate any possible signal amplitude distortions due to limited filter bandwidths. A 30-sample LLID time domain sequence, whose absolute amplitude values are set to 1000, is inserted in the frame’s header for ONU identification and detected by amplitude decision in the time domain. In the LLID sequence, three adjacent samples are taken each time to represent one bit, thus 10 bits can be obtained using the 30 samples. Actually, to achieve the DC-balanced high-speed channels, the 10-bit LLID is obtained from an 8-bit sequence encoded by an 8B/10B encoder, thus a total number of 256 ONUs can be accommodated. Following the LLID sequence are two FFT-sized sampling training sequences (TSs) and  $M$  data-carrying OFDM symbols.

Corresponding to the abovementioned frame structure in Fig. 3(a), the time-domain waveform of the LLID sequence of “1010101010” captured at a received optical power of -10 dBm is shown in Fig. 3(b). The amplitude threshold for LLID identification is set to 80, because our previous work [5] has experimentally proved that such an amplitude threshold can achieve 100% LLID recognition accuracy. Due to the limited filter bandwidth, the values of the first and third samples of the captured three samples representing a bit are smaller than that of the second sample. Therefore, in this paper, the value of the second sample is used to represent the recognition result of the bit in the LLID identification. And due to the reverse effect of the physical design adopted in this paper, as shown in Fig.3(b), the 1<sup>st</sup> bit is judged to be logic 1 if its corresponding amplitude is lower than -80 and the 10<sup>th</sup> bit is judged to be logic 0 if its



corresponding amplitude value is higher than 80.

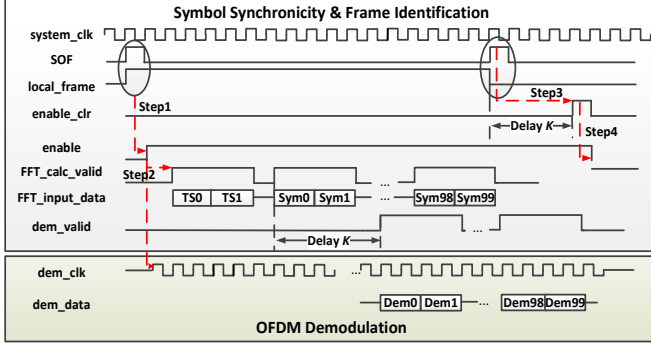


Fig. 4. Implementation of the clock-gating scheme in physical layer.

### C. Implementation of the clock-gating scheme in physical layer

To demonstrate the proposed technique in a FPGA, the important signals used in the clock-gating-based energy-saving scheme are presented in Fig. 4. The “start of the frame (SOF)” signal is generated by the frame alignment module and used to indicate the start of an OFDM frame, i.e. when a frame arrives, it is set to high and maintains the status for one clock period. The “local\_frame” signal is used to indicate the result of frame identification and is set to high when the received frame is for the destination ONU, otherwise it is set to low. The “enable” signal is triggered if both the “SOF” signal and the “local\_frame” signal are high at the rising edge of the system clock. When the enable signal is active, the corresponding OFDM demodulation module clock (i.e. gating clock) named “dem\_clk” is output by BUFGE to ensure the normal operation of the OFDM demodulation module, as shown in Fig. 4. To overcome the influence of the demodulation clock’s instability on the OFDM demodulation performance, the “FFT\_calc\_valid” signal and the corresponding sampled realignment ADC data, i.e., the “FFT\_input\_data” signal (used for the real-time FFT operation), are delayed by one clock period after the set of the “enable” signal. Given the fact that the pipeline processing is implemented for the demodulation module and the pipeline delay is fixed at  $K$  clock periods, the indication signal, which is named “dem\_valid” and used to indicate the result of OFDM demodulation in Fig. 4, needs to be generated after the  $K$  clock delay from the “FFT\_calc\_valid” signal. In Fig. 4, the “dem\_valid” signal is generated from the frame identification module in the system clock domain, which is different from the traditional scheme. Such a technique ensures that the MAC layer operation is not relevant to the clock on/off state in physical layer, this enormously reduces the complexity of the hardware designs.

Because of the pipeline delay induced by the demodulation module, the “enable” signal of the clock-gating module should not be set to low immediately after the received frame is recognized as a non-local frame because the previous frame is not fully demodulated yet. To cope with such a situation, a signal named “enable\_clr”, which is used to set the “enable” signal invalid, is set to high after the  $K$  clock delay if the newly obtained OFDM frame is not for the ONU.

### D. Theoretical Analysis of FPGA chip power consumption and energy-saving efficiency of an ONU’s OFDM receiver

The power consumption of a FPGA chip at the receiver side includes two parts: static power consumption and dynamic power consumption. In this paper, the static power consumption is defined as the energy consumption of a FPGA chip when the “enable” signal is set to low, i.e. the clock of the demodulation module is deactivated; and the dynamic power consumption refers to the remaining power consumption of the chip excluding the static power consumption part. In this subsection, we discuss the FPGA chip power consumption for cases of a single ONU and multiple ONUs for the downlink unicast scenario.

#### 1) Chip power consumption of an OFDM receiver for the single ONU case

For the single ONU case (point-to-point transmission system), the ratio of a local frame, i.e. traffic load, is a key factor determining the dynamic power consumption part, the ratio is written as:

$$\alpha = \frac{n}{m}, \quad (n \leq m) \quad (1)$$

where  $n$  is the number of local frames and  $m$  is the number of received total frames during an observation period. Then the total energy consumption of a FPGA chip is given by:

$$P_{total} = (\alpha + \beta) \times P_D + P_S \quad (2)$$

where  $P_S$  is the aforementioned static power consumption,  $P_D$  is the maximum dynamic power consumption measured when the “enable” signal is always set to high, and  $\beta$  is the correction factor which corrects the power induced by the pipeline delay of  $K$  clocks.  $\beta$  is related to traffic load  $\alpha$  and time of frame demodulation  $T_{Dem}$ . For different values of traffic load  $\alpha$ , the maximum value of  $\beta$  can be expressed as:

$$\beta = \begin{cases} \alpha \times \gamma \times \frac{K \times T_{clk}}{T_{Dem}}, & 0 \leq \alpha \leq 50\% \\ (1 - \alpha) \times \gamma \times \frac{K \times T_{clk}}{T_{Dem}}, & 50\% < \alpha \leq 100\% \end{cases} \quad (3)$$

where  $T_{Dem}$  is the time duration of each OFDM frame demodulation, and  $T_{clk}$  is the period of the system clock. Considering the fact that the power of the FPGA chip during the pipeline delay period is slightly lower than the power consumed during OFDM demodulation, so  $\beta$  needs an additional correction factor, denoted as  $\gamma$ . When  $\alpha$  is less than 50%, the number of the non-local frames is more than the number of the local frames, so we set all the local frames discontinuous to maximize the value of  $\beta$  for the corresponding traffic load; otherwise we set all the non-local frames discontinuous to maximize  $\beta$ .

After the OFDM receiver is designed, its static power consumption  $P_S$  and the maximum dynamic power consumption  $P_D$  are also determined consequently, both of which can be considered as constants. From Eq. (2) and Eq. (3) it can be understood that when the traffic load  $\alpha$  is the main factor affecting the power consumption and they are positively correlated, when the traffic load is 0, the power consumption of the FPGA chip is the lowest and only the static power

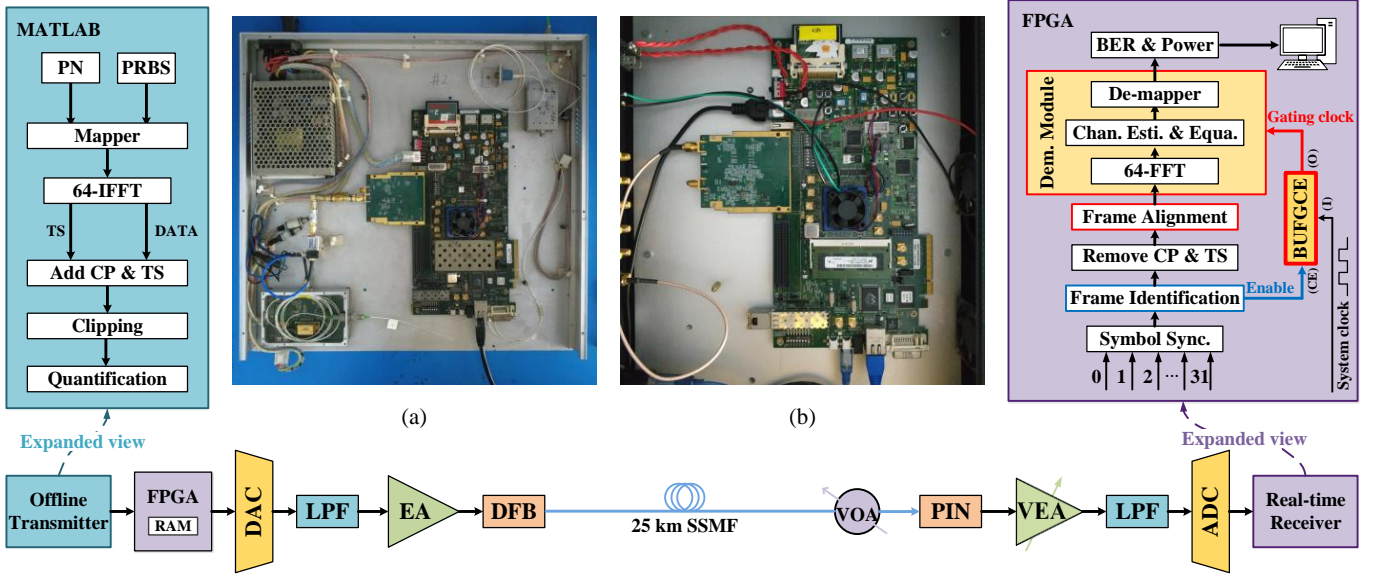


Fig. 5. Experimental system and transceiver DSP blocks of real-time OFDM-PON. (a) Transmitter based on Xilinx ML605 FPGA board; (b) real-time receiver based on Xilinx ML605 FPGA board.

consumption exists, which is determined by the chip-manufacturing process. On the other hand, when the traffic load is 100%, the values of  $\alpha$  and  $\beta$  are 1 and 0, respectively, therefore the FPGA chip operates at its highest power consumption state.  $\beta$  is a correction factor of the FPGA chip power, which can be reduced by two ways: the first is to increase the value of  $T_{Dem}$  by increasing the data-carrying symbols per OFDM frame, and the second is to reduce the pipeline delay time through designing a more efficient FFT FPGA implementation. Since the pipeline delay of the considered demodulation module is fixed at 55 clock periods, the influence of  $\beta$  on power consumption can be reduced by choosing an appropriate frame length.

#### 2) Energy-efficiency in multiple ONU case

In a unicast downlink OFDM PON consisting of multiple ONUs (point-to-multi-point transmission system), assuming that there are  $N$  ONUs communicating with one OLT, and the total downlink traffic load for these ONUs is  $\alpha$  and the traffic load is evenly distributed among these ONUs, so the traffic load of each ONU, denoted by  $\alpha'$ , is  $\alpha/N$ . Because the number of ONUs in the PON system is greater than 1, the traffic load of each ONU does not exceed 50% provided that the traffic load is evenly distributed among these ONUs. Let  $P_{total}^N$  denote the total power consumption of  $N$  ONUs in the clock-gating scheme, then we have

$$P_{total}^N = N \times P_S + N \times (\alpha' + \beta) \times P_D, \quad \alpha' = \frac{\alpha}{N} \quad (4)$$

In the conventional scheme, all the ONUs need to demodulate all the received OFDM frames, so the total power consumption of the receivers is  $N \times P_{Con}$ , where  $P_{Con}$  is the FPGA chip power consumption of each ONU in the conventional scheme. Therefore, the energy-efficiency of the energy-saving scheme can be written as:

$$\begin{aligned} \eta &= 1 - \frac{P_{total}^N}{N \times P_{Con}} \\ &= 1 - \frac{P_S}{P_{Con}} - \frac{\alpha}{N} \left( 1 + \frac{K \times T_{clk}}{T_{Dem}} \right) \frac{P_D}{P_{Con}} \end{aligned} \quad (5)$$

From Eq. (4) and Eq. (5) it can be seen that the energy-saving efficiency is negatively correlated with total traffic load  $\alpha$  and

correction factor  $\beta$ , and positively correlated with ONU count. When the total traffic load and the frame length are fixed, the energy-saving efficiency decreases with increasing ONU count and eventually tends to a stable value, i.e.  $1 - P_S/P_{Con}$ .

#### IV. EXPERIMENTAL SETUP

To verify the energy-saving efficiency of the proposed clock-gating-based energy-saving scheme, experiments are undertaken using a FPGA-based real-time IMDD OFDM PON platform, as shown in Fig. 5. In this paper, two Xilinx FPGA boards named ML605 with Virtex-6 XC6VLX240T are used in the implementation of the OFDM PON platform. The key parameters of the transceiver are summarized in Table I.

At the OFDM transmitter side, the OFDM modulation is completed off-line by MATLAB software, including pseudo-random binary sequence (PRBS) generation, constellation mapping, IFFT operation, cyclic prefix (CP) and training sequence (TS) insertions, quantization and ~12 dB clipping.

TABLE I  
OFDM-PON SYSTEM PARAMETERS

Parameter	Value
FFT/IFFT points	64
Data-carrying subcarriers	From 2 to 28
Modulation format	2/4/8/16/32/64-QAM
ADC/DAC resolution	10/12-bit
ADC& DAC sample rate	4 GS/s
OFDM frame CP	16 samples (4 ns)
PRBS	$2^{15} - 1$
Transmitter output power	+ 7.75 dBm
DFB wavelength	1549.98 nm
DFB modulation bandwidth	2.7 GHz
DFB bias current	45 mA
DFB driving voltage	2 Vpp
PIN detector bandwidth	40 MHz ~ 3 GHz
PIN responsivity	0.9 mA/mW

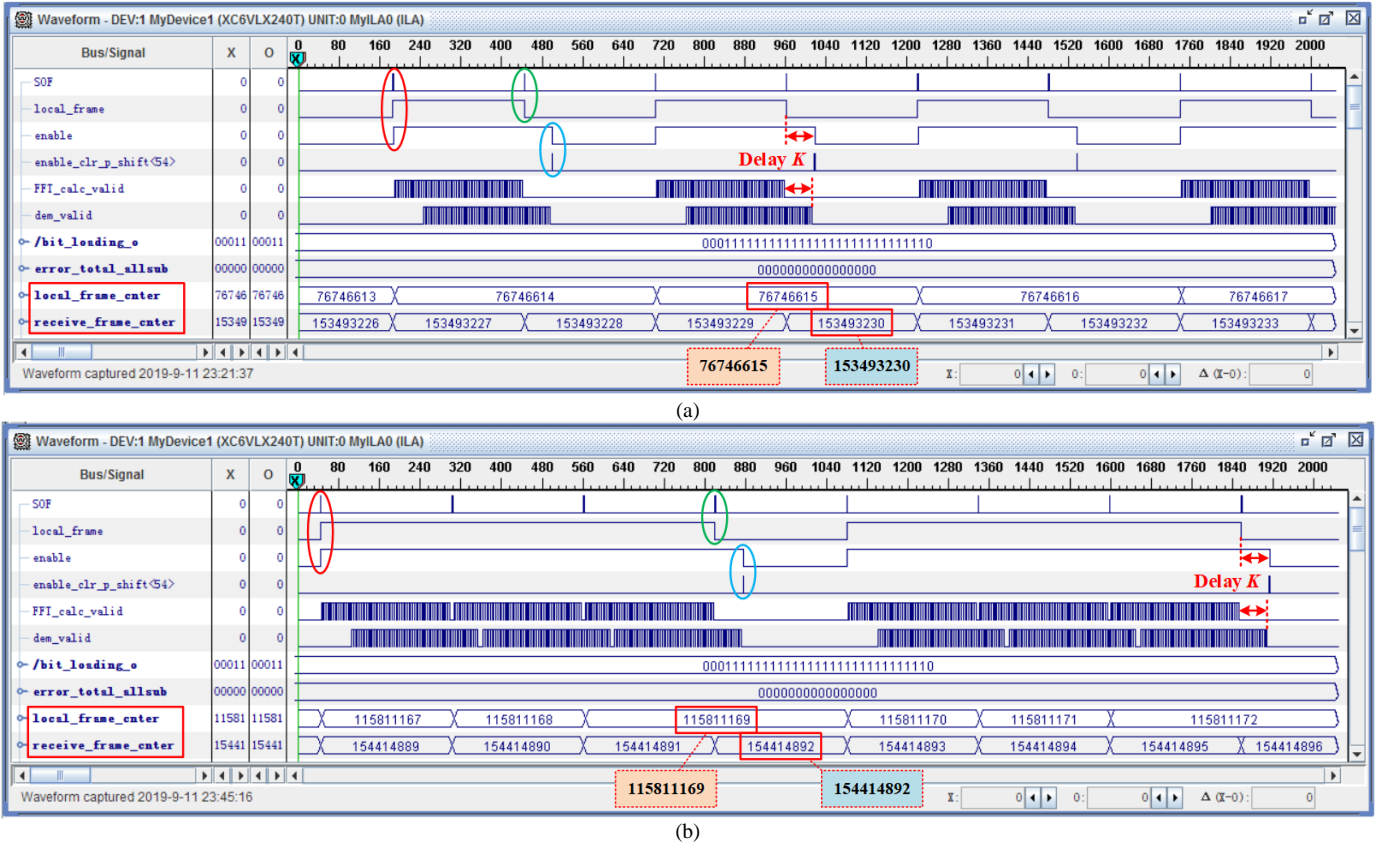


Fig. 6. The control signals for clock-gating scheme in Chipscope analyzer (ROP = -10 dBm, BPSK, 100 symbols/frame). (a) 50% traffic load; (b) 75% traffic load.

The FFT size is set to be 64, and the signal modulation formats vary between BPSK, 4-QAM, 8-QAM, 16-QAM, 32-QAM and 64-QAM. To overcome the channel's low-pass frequency response and ADC roll-off effects, the first two and last three subcarriers are turned off and the remaining subcarriers are used to carry data. In order to obtain real-valued IFFT outputs, all of the encoded subcarriers needs to satisfy the Hermitian symmetry. After the 64-point IFFT operation, a 16-sample cyclic prefix, two FFT-sized sample TSs, and  $M$  OFDM symbols carrying data are inserted, in the time domain, to form a complete OFDM frame. And then the generated OFDM frames after 12-bit quantization are transmitted to the internal RAM of the Xilinx ML605 FPGA board equipped with a 4 GS/s @ 12-bit DAC by UDP transport protocol, as shown in Fig. 5(a). The electrical analog signal output by the DAC is fed to a narrow bandwidth distributed feedback laser (DFB-LD) via a 2 Vpp variable attenuator and a 13 dB amplifier to modulate the baseband OFDM signal onto the optical carrier, which is then injected into a 25 km standard single-mode fiber (SSMF).

At the receiver side, firstly, a variable optical attenuator (VOA) is used to adjust the received optical power and the optical signal is then converted to the electronic domain via a 2.7 GHz PIN detector. A variable electrical amplifier (VEA) amplifies the electrical OFDM signal to ensure that the signal occupies the full dynamic range of the 10-bit ADC, which converts the received analog electrical OFDM signal into the digital domain. After high-speed sampling, the digital signals are first de-multiplexed into 32-parallel samples, and the receiver performs synchronization by utilizing the leading zeros

shown in Fig. 3(a). Then the receiver performs LLID identification described in Section III. When symbol synchronization and LLID identification are completed, two training sequences for channel estimation and a CP of 16 samples at the beginning of each OFDM symbol are removed, followed by subsequent DSP procedures including 64-point FFT, channel equalization and de-mapping to achieve OFDM demodulation. It should be noted that the FFT module in our real-time OFDM receiver is generated by using online Spiral DFT/FFT IP Core Generator provided by Carnegie Mellon University and the bit resolution is set to be 16. The demodulated OFDM symbols are then transmitted to a real-time BER calculator, where the received data is compared with the transmitted PRBS sequence. All of these DSP functions are performed in the real-time OFDM receiver, as shown in Fig. 5(b). The directly modulated DFB laser incorporated in the above-described platform can be easily replaced with other light sources such as directly modulated weak-resonant-cavity laser diode (WRC-FPLD) [16], and a directly modulated antireflection coated Fabry–Perot laser amplifier [17].

To accurately measure the chip power consumption, an adapter called USB-TO-GPIO is used to show online the power from UCD9240, a digital power controller on the ML605 FPGA board, via a PMBus command protocol at the receiver.

## V. EXPERIMENTAL RESULTS

### A. Real-time experimental verification of the high reliability and accuracy of control signals for the clock-gating module

To verify the reliability and accuracy of the control signals



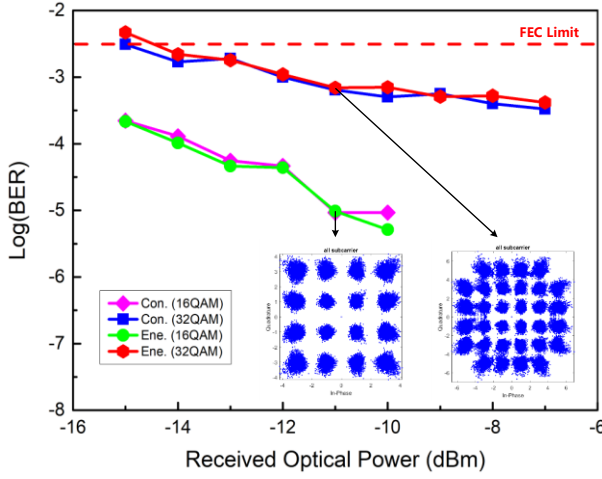


Fig. 7. Real-time measured BER versus received optical power with different modulation formats for the conventional (Con.) and clock-gating (Ene.) schemes (100 symbols/frame).

for the clock-gating scheme, some key signals are captured by the Chipscope analyzer provided by Xilinx software in our real-time experiments where  $\alpha$  is set to 50% and 75% which are shown in Fig. 6(a) and Fig. 6(b), respectively. In experimentally measuring Fig. 6(a) and Fig. 6(b), the received optical power is set at -10 dBm and the BPSK modulation format is chosen to ensure that zero BERs without clock-gating control are still observed in order to evaluate the accuracy of the clock-gating control.

As shown in Fig. 6, as expected, when a local frame arrives, the “local\_frame” signal is set to be high immediately, and then the “enable” signal is also raised to high, as shown in the red oval box, to enable the clock needed for OFDM demodulation. It is clear that if the next frame is non-local and the current one is local, the “local\_frame” signal is set to be low immediately, as shown in the green oval box of Fig. 6. Thus, the “local\_frame” signal can be used directly to distinguish whether the received OFDM frame is local or not. However, as stated in section III.B, the “enable” signal controlling the CE port of the BUGCE module is not immediately set to be low, as the OFDM demodulation process has not been finished even if the next frame is not local frame. In our OFDM receiver FPGA design, the pipeline delay  $K$  is 55 and the corresponding “enable” signal is set to be low after 55 clock delay from the moment that the “local\_frame” signal is set to be low, as shown in the blue oval box in Fig. 6. And the “dem\_valid” signal used to indicate the validity of the OFDM demodulation process is also delayed by 55 clocks accordingly, as shown in Fig. 6. Therefore, the excellent consistency between the experimental results and the proposed principle of the implemented clock-gating scheme control presented in section III.C, verifies the feasibility of utilizing only one BUGCE to control the on/off state of the operation clock for OFDM demodulation.

To further verify the accuracy and reliability of the control signals, at the transmitter side, the traffic load is taken to be 50% and 75%, corresponding each of which experimental measurements are undertaken, in a statistical manner, at the receiver side. In Fig. 6, the signal “local\_frame\_cnter” is used to count the number of identified local frames, whereas the

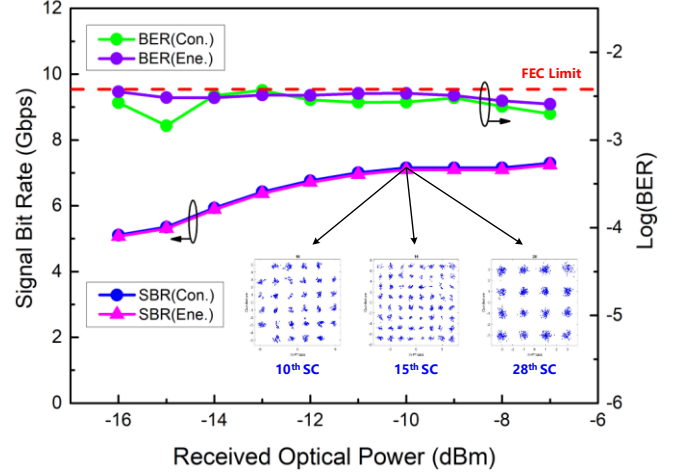


Fig. 8. Signal bit rate and real-time BER for the conventional and clock-gating schemes using adaptive bit loading (100 symbols/frame).

“receive\_frame\_cnter” signal is used to count the number of all received frames, and the ratio of these two is the traffic load experimentally measured at the receiver. From Fig. 6 it can be seen that, at the receiver side, the ratio of the number of identified local frame (“local\_frame\_cnter” signal) to the total number of received frames (“receive\_frame\_cnter” signal) is 50% and 75% respectively, which is consistent with the traffic load set at the transmitter. It should be pointed out that the sequence numbers of the identified local and non-local frames are also exactly the same compared to those set at the transmitter. This indicates that there are no missing frames in frame identification. In addition, the “error\_total\_allsub” signal, which is used to count the cumulative error bits for all subcarriers in Fig. 6, is 0, indicating that there is no bit error in all the received local frames. Therefore, the high reliability and accuracy of the clock-gating scheme are fully verified in the real-time OFDM platform.

#### B. Real-time experimental verification of negligible transceiver performance degradations caused by the clock-gating scheme

Having identified the high control accuracy of the clock-gating scheme in the real-time FPGA-based OFDM-PON platform, in this subsection, attention is focused on experimentally demonstrating negligible transceiver performance degradations caused by the clock-gating scheme. The measured real-time BER performance against received optical power for different modulation formats for both the conventional scheme (abbreviated as Con.) and the clock-gating scheme (abbreviated as Ene.) are depicted in Fig. 7, where identical signal modulation formats are adopted for all the data-carrying subcarriers. As expected, it can be seen in Fig. 7 that, for various received optical powers and different modulation formats, the transceiver BER performances with the clock-gating scheme are almost identical to the traditional scheme where the clock is always activated. It should also be noted that a 50% traffic load is adopted to measure the BER performance for the clock-gating scheme and that 150,000 OFDM frames are counted to measure the BER performance for the aforementioned two cases. The forward error correction (FEC) limit adopted in this paper is  $3.8 \times 10^{-3}$ . For the clock-

gating energy-saving scheme, the 16-QAM and 32-QAM constellation diagrams measured at received optical powers of -11 dBm are also given in Fig. 7.

Since adaptive bit loading is always applied on each individual subcarrier to ensure that a maximized throughput is achieved, the experimental measured transceiver BER and signal bit rate as a function of received optical power is plotted in Fig. 8. As the same adaptive bit loading profile is adopted for the clock-gating scheme and the traditional scheme, the achievement of the almost identical signal bit rates is expected. As also shown in Fig. 8, the negligible transceiver BER performance degradations over a wide range of received optical powers indicate the effectiveness, validity and precision of the proposed clock-gating scheme for practical applications. The constellation diagrams of the 10<sup>th</sup>, 15<sup>th</sup> and 28<sup>th</sup> subcarriers under the clock-gating energy-saving scheme at a received optical power of -10 dBm are also given in Fig. 8.

### C. Analysis of the energy-efficiency of the clock-gating scheme

Before analyzing the energy-efficiency of the proposed clock-gating scheme, it is very important to experimentally obtain the static and dynamic powers for the adopted ML605 FPGA board performing real-time OFDM demodulation. In this paper, by setting the traffic load  $\alpha$  to 0, the measured ML605 power is 2.28 W, referred to as static power consumption  $P_S$  where the clock for OFDM demodulation is always deactivated. Whilst the measurement of the dynamic power is undertaken by subtracting the static power from the total power, thus, the dynamic power can be worked out to be 2.63W, as the measured FPGA board power is 4.91W by setting the traffic load  $\alpha$  to 1 where the clock for OFDM demodulation is always on.

#### 1) Experimental verification of the high energy efficiency for the single ONU case

The experimentally measured FPGA power consumption as a function of traffic load is plotted in Fig. 9 for a point-to-point transmission system. In obtaining Fig. 9, the traffic load is controlled at the transmitter side by adjusting the ratio of the LLID used for the ONU, and the number of symbols used for the OFDM frame is set to 100.

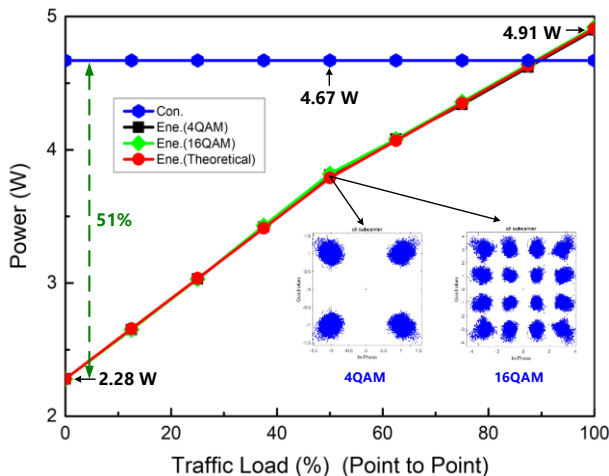


Fig. 9. Theoretical and experimental measured FPGA power consumption of clock-gating scheme in different traffic load (-10 dBm, 100 symbols/frame).

In Fig. 9, three important aspects should be highlighted: firstly, for fixed traffic loads, the FPGA power consumption is independent of modulation format, as the required FPGA logic resource to perform the OFDM demodulation is the same for the 4-QAM and 16-QAM cases. This implies that reducing the FPGA resource usage is an effective approach to decrease the FPGA power consumption. Secondly, for higher traffic loads of >87%, the power consumption associated with the clock-gating scheme is 0.24W higher than the traditional scheme, as an additional FPGA logic resource is induced to accurately control the gating clock. Moreover, considering the fact that the average traffic load is less than 50% for a point-to-multi-point case which is always used for the practical case stated in next subsection, such an additional power consumption does not have any real impacts. Thirdly, the experimentally measured FPGA power consumption agrees well with the theoretical results predicted by Eq. (2) (red line). This indicates that Eq. (2) can be used to calculate the chip power consumption for the point-to-point transmission system and also provides a theoretical basis for simulating the power consumption for point-to-multi-point transmission systems. In obtaining the theoretical results in Fig. 9, the value of  $K \times T_{clk}/T_{Dem}$  is 0.21, by considering the fact that the number of OFDM symbols per frame is 100 and the pipeline delay is 55, and  $\gamma$  is 0.7 which is measured experimentally.

The relationship between  $\beta$  and the power consumption is also explored by changing the number of OFDM symbols within each frame, the resulting experimentally measured curves of the FPGA power consumptions with different frame lengths for three traffic loads are plotted in Fig. 10, which shows two useful features: Firstly, the three curves obtained by the experimental measurements are in excellent agreement with the theoretical curves calculated using Eq. (2) and Eq. (3). This implies that the power consumption model still holds well even if variable OFDM symbols are utilized in the real-time OFDM PON platform. Secondly, with increasing the number of OFDM symbols, the power consumption of the FPGA chip decreases sharply until a stable value is reached. This is because when the number of symbols is small, the value of  $\beta$  is large, and the power consumption caused by the pipeline delay cannot be ignored, thus giving rise a large symbol number-induced sharp

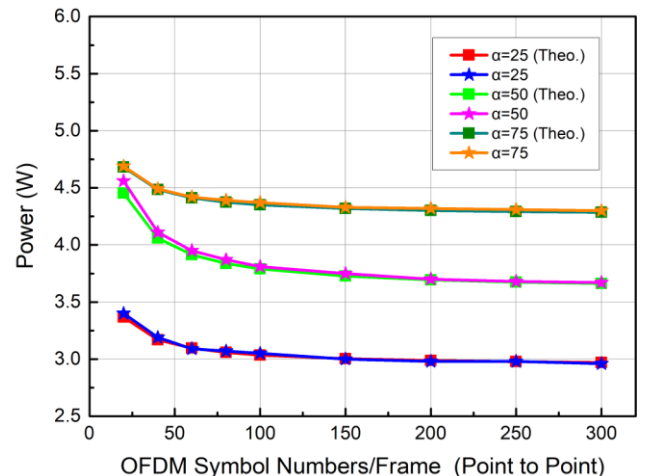


Fig. 10. Theoretical and experimental measured FPGA power consumption of clock-gating scheme in various frame length (-10 dBm, 4-QAM).

reduction in chip power consumption. On the other hand, when the number of OFDM symbols is greater than 100, the value of  $\beta$  is small, and the power consumption caused by the pipeline delay can be ignored. Thus the minimum duration of one OFDM frame, i.e., the control granularity of the operating clock is about 2  $\mu$ s, taking into account that an 125MHz clock is used to perform the OFDM demodulation in the ML605 FPGA platform.

To highlight the power-saving merits compared with our previous work [5], comparisons of power consumption between the clock-gating scheme, the toggle-rate scheme and the conventional scheme in the point-to-point transmission system are listed in Table II, where all the received OFDM frames are non-local. Table II shows that the clock-gating-based scheme can save 51% power compared with the conventional scheme, and 29% power compared with our previous work [5]. The clock-gating scheme is more energy efficient than the toggle-rate scheme because the latter one sets only the sampling data of the non-local frames to zero to reduce the toggle-rate but the demodulation clock is still on; while in the clock-gating scheme, the demodulation clock is off to further lower the dynamic power consumption, so the clock-gating scheme can achieve a higher energy-saving efficiency.

TABLE II  
MEASURED FPGA POWER CONSUMPTION ( $\alpha = 0$ )

Item	Power consumption (W)	Energy saving ratio
Conventional	4.67	51%
Toggle-rate based [5]	3.19	29%
Clocking-gating based	2.28	/

## 2) Experimental verification of energy efficiency for the multiple ONUs case

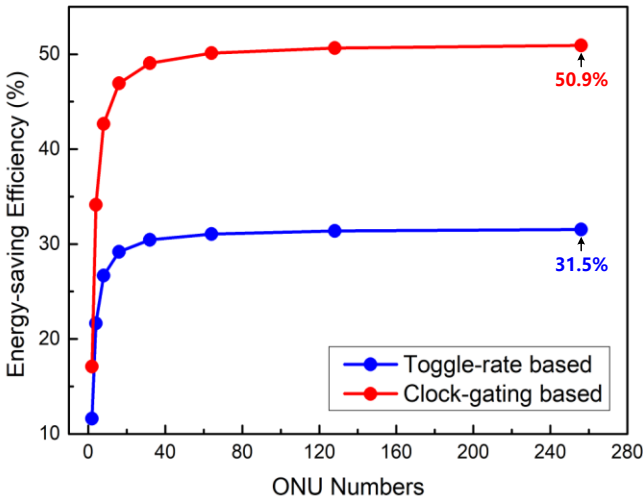


Fig. 11. Energy-saving efficiency of clock-gating and toggle-rate scheme with different ONUs.

In Fig. 11, by making use of Eq.(5), the simulated energy efficiency for the clock-gating and toggle-rate schemes for the unicast downlink multiple ONU PON are depicted, where the total downlink traffic load for all ONUs  $\alpha$  is set to be 100%. From Fig. 11, it can be seen that as the number of ONUs increases, the slope of these two energy-saving efficiency curves gradually decreases and finally reaches to zero, because

the value of the third item in Eq. (5) becomes smaller and smaller, and finally reaches zero. The energy-saving efficiency can be up to 50.9%, which is very close to its theoretical limit of 51% for the clock-gating scheme when the number of ONUs are 256. For the considered case, the total chip power consumption is dominated by the static power, which is determined by the chip-manufacturing process. The overall energy-saving efficiency of the clock-gating scheme is more significant than the toggle-rate scheme.

## VI. CONCLUSIONS

In this paper, a novel clock-gating-based energy-efficient scheme applicable in ONUs in OFDM-PONs has been proposed for the first time, which performs the selective reception of OFDM frames in the downlink. In the proposed scheme, a simple clock-gating module named BUFGCE is used to control the clock of a demodulation module according to the frame recognition outputs. For a downlink unicast OFDM-PON scenario, when an OFDM frame arrives, only the target ONU's demodulation clock is activated for OFDM demodulation, while the demodulation clocks of all the remaining ONUs are deactivated to keep those ONUs in their lowest power consumption states.

Experiments have been undertaken in our real-time IMDD OFDM-PON platform, and the measured results have shown that up to 51% power consumption of a FPGA chip in the ONUs can be saved compared to conventional OFDM-PONs in downlink unicast scenarios. It has also been verified that the control signals in the clock-gating module is highly accurate and reliable, and causes negligible transceiver performance degradations. Moreover, the proposed clock-gating energy-saving scheme does not need additional clock recovery circuits and higher-layer scheduling controls for achieving the high energy-saving efficiency. In addition, the proposed scheme can also be easily integrated with other energy-saving solutions of low FPGA DSP complexity.

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